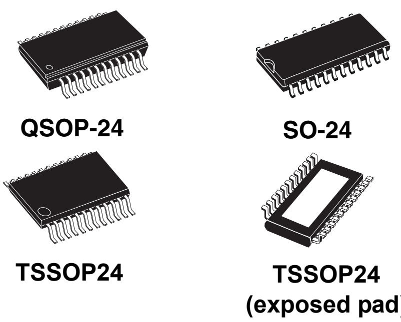
STP16CPC05

Low voltage 16-bit constant current LED sink driver with balanced output rise/fall time

Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Can be driven by a 3.3 V microcontroller
- Output current: 5-100 mA
- Max clock frequency 30 MHz
- ESD protection 2.5 kV HBM, 200 V MM



Description

The STP16CPC05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CPC05 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 5 mA to 100 mA constant current to drive the LEDs.

The STP16CPC05`s output stage is designed to optimize the turn-on and turn-off time, typically 100 nS. The balanced turning ON/OFF improves the system performances reducing the bypass capacitance in applications where parasitic inductance generate ringing or noise in the system. The LEDs' brightness can be controlled by using an external resistor to adjust the STP16CPC05 output current.

The STP16CPC05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series.The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is useful in applications that interface with a 3.3 V microcontroller.

Table 1. Device summary

Order codes	Package	Packaging
STP16CPC05MTR	SO-24	1000 parts per reel
STP16CPC05TTR	TSSOP24	2500 parts per reel
STP16CPC05XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPC05PTR	QSOP-24	2500 parts per reel

Contents

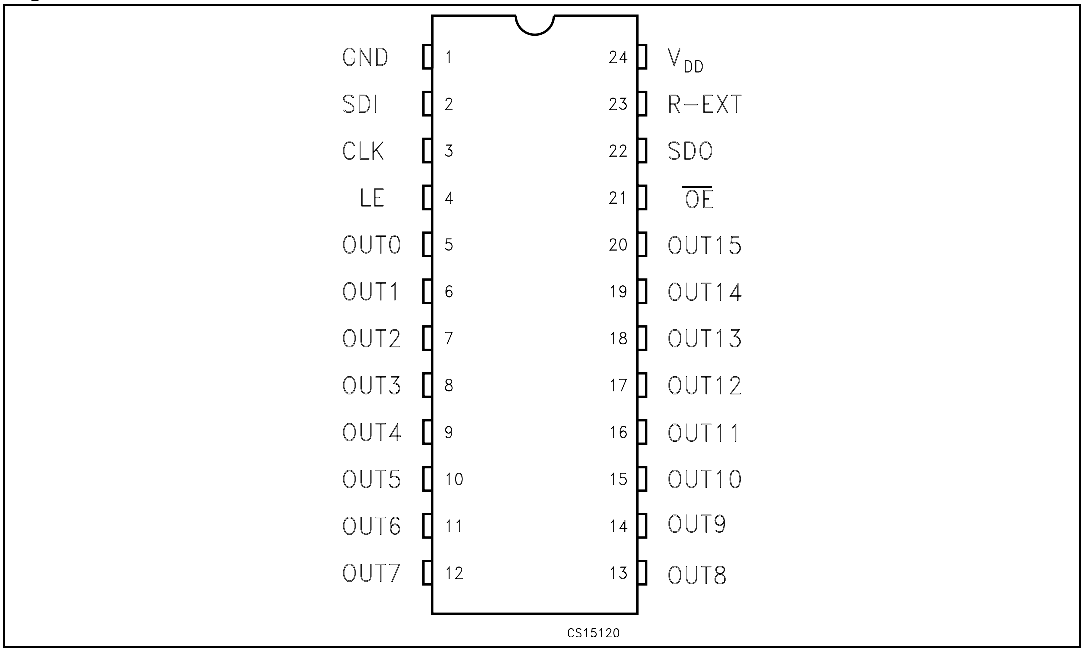
1 Summary description

Table 2. Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	±1.5%	±5%	≥ 20 to 100 mA	3.3 V to 5 V	25 °C

1.1 Pin connection and description

Figure 2. Pin connection



Note: Exposed-pad should be electrically connected to a metal land electrically isolated or connected to ground

Table 3. Pin description

Pin N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	100	mA
V_I	Input voltage	-0.4 to V_{DD}+0.4	V
I_{GND}	GND terminal current	1600	mA
f_{CLK}	Clock frequency	50	MHz

2.2 Thermal data

Table 5. Thermal data

<table>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Value</th><th>Unit</th></tr>
<tr><td>T_{OPR}</td><td colspan="2">Operating temperature range</td><td>-40 to +125</td><td>°C</td></tr>
<tr><td>T_{STG}</td><td colspan="2">Storage temperature range</td><td>-55 to +150</td><td>°C</td></tr>
<tr><td rowspan="4">R_{thJC}</td><td rowspan="4">Thermal resistance junction-case</td><td>SO-24</td><td>60</td><td>°C/W</td></tr>
<tr><td>TSSOP24</td><td>85</td><td>°C/W</td></tr>
<tr><td>TSSOP24[(1)]
exposed pad</td><td>37.5</td><td>°C/W</td></tr>
<tr><td>QSOP-24</td><td>72</td><td>°C/W</td></tr>
</table>

1. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

2.3 Recommended operating conditions

Table 6. Recommended operating conditions T_A = 25 °C

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3.0	-	5.5	V
V_O	Output voltage			-	20	V
I_O	Output current	OUTn	3	-	100	mA
I_{OH}	Output current	SERIAL-OUT		-	+1	mA
I_{OL}	Output current	SERIAL-OUT		-	-1	mA
V_{IH}	Input voltage		$0.7V_{DD}$	-	$V_{DD}+0.3$	V
V_{IL}	Input voltage		-0.3	-	$0.3V_{DD}$	V
t_{wLAT}	LE pulse width	V_{DD} = 3.3 V to 5.0 V	20	-		ns
t_{wCLK}	CLK pulse width		16	-		ns
t_{wEN}	$\overline{OE}$ pulse width		200	-		ns
$t_{SETUP(D)}$	Setup time for DATA		8	-		ns
$t_{HOLD(D)}$	Hold time for DATA		4	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		5	-		ns
f_{CLK}	Clock frequency	Cascade operation (1) V_{DD} = 5 V		-	30	MHz

1. If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please considered the timings carefully.

3 Electrical characteristics

V_{DD} = 3.3 V to 5 V, T_A = 25 °C, unless otherwise specified

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage high level		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input voltage low level		GND		$0.3V_{DD}$	V
I_{OH}	Output leakage current	V_{OH} = 20 V			10	µA
V_{OL}	Output voltage (Serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (Serial-OUT)	I_{OH} = -1 mA	V_{DD}-0.4V			V
I_{OL1}	Output current	V_O = 0.3 V, R_{ext} = 4.2 kΩ	4.25	5	5.75	mA
I_{OL2}		V_O = 0.3 V, R_{ext} = 1 kΩ	19	20	21	
I_{OL3}		V_O = 1.3 V, R_{ext} = 200 Ω	96	100	104	
ΔI_{OL1}	Output current error between bit (All Output ON)	V_O = 0.3 V, R_{ext} = 4.2 kΩ		± 5	± 8	%
ΔI_{OL2}		V_O = 0.3 V, R_{ext} = 1 kΩ		± 1.5	± 3	
ΔI_{OL3}		V_O = 1.3 V, R_{ext} = 200 Ω		± 1.2	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	kΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	kΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{EXT} = 1 kΩ OUT 0 to 15 = OFF		4		mA
$I_{DD(OFF2)}$		R_{EXT} = 250Ω OUT 0 to 15 = OFF		11.2		
$I_{DD(ON1)}$	Supply current (ON)	R_{EXT} = 1 kΩ OUT 0 to 15 = ON		4.5		
$I_{DD(ON2)}$		R_{EXT} = 250Ω OUT 0 to 15 = ON		11.7		
Thermal	Thermal protection			170		°C

V_{DD} = 5 V, T_A = 25 °C, unless otherwise specified

Table 8. Switching characteristics

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
t_{PLH1}	Propagation delay time, CLK-$\overline{OUTn}$, LE = H, $\overline{OE}$ = L	$V_{IH} = V_{DD}$ V_{IL} = GND I_O = 20 mA R_{EXT} = 1 kΩ C_L = 10 pF V_L = 3.0 V R_L = 60 Ω	V_{DD} = 3.3 V	-	175	227	ns
			V_{DD} = 5 V	-	159	206	
t_{PLH2}	Propagation delay time, LE-$\overline{OUTn}$, $\overline{OE}$ = L		V_{DD} = 3.3 V	-	176	228	ns
			V_{DD} = 5 V	-	158	205	
t_{PLH3}	Propagation delay time, $\overline{OE}$-$\overline{OUTn}$, LE = H		V_{DD} = 3.3 V	-	235	305	ns
			V_{DD} = 5 V	-	192	250	
t_{PLH}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	20	26	ns
			V_{DD} = 5 V	-	14	18	
t_{PHL1}	Propagation delay time, CLK-$\overline{OUTn}$, LE = H, $\overline{OE}$ = L		V_{DD} = 3.3 V	-	70	91	ns
			V_{DD} = 5 V	-	68	88	
t_{PHL2}	Propagation delay time, LE-$\overline{OUTn}$, $\overline{OE}$ = L		V_{DD} = 3.3 V	-	56	73	ns
			V_{DD} = 5 V	-	54	70	
t_{PHL3}	Propagation delay time, $\overline{OE}$-$\overline{OUTn}$, LE = H		V_{DD} = 3.3 V	-	102	132	ns
			V_{DD} = 5 V	-	100	130	
t_{PHL}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	25	32	ns
			V_{DD} = 5 V	-	17	22	
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V	-	116	150	ns
			V_{DD} = 5 V	-	108	140	
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V	-	80	104	ns
			V_{DD} = 5 V	-	80	104	
t_r	CLK rise time [(1)]			-		5000	ns
t_f	CLK fall time [(1)]			-		5000	ns

1. In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

4 Equivalent circuit and outputs

Figure 3. $\overline{OE}$ terminal

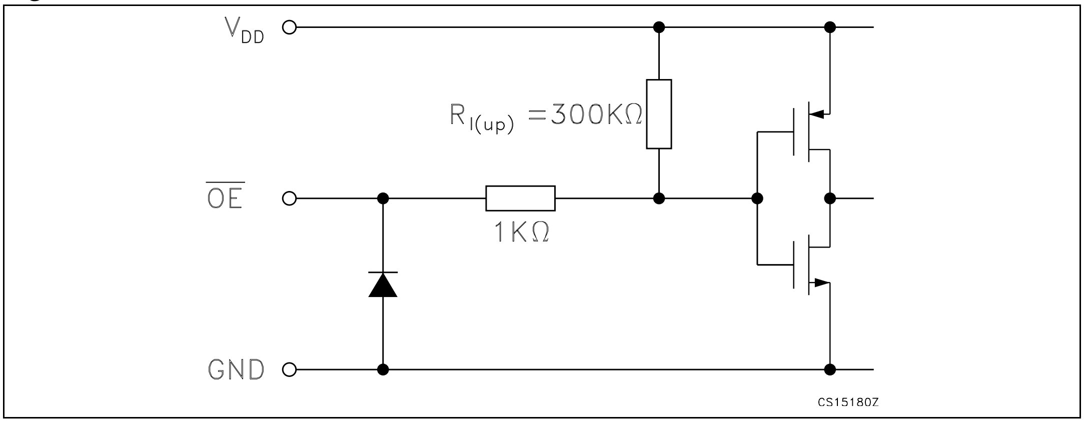


Figure 4. LE terminal

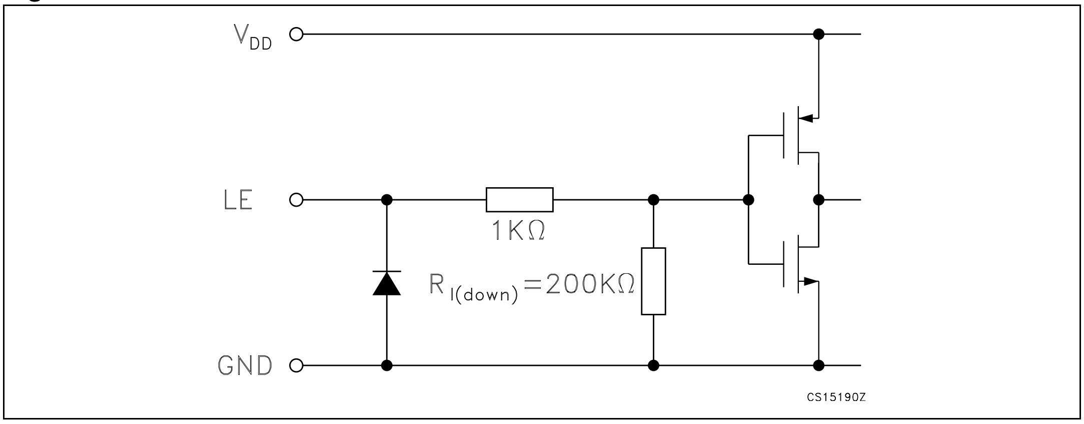


Figure 5. CLK, SDI terminal

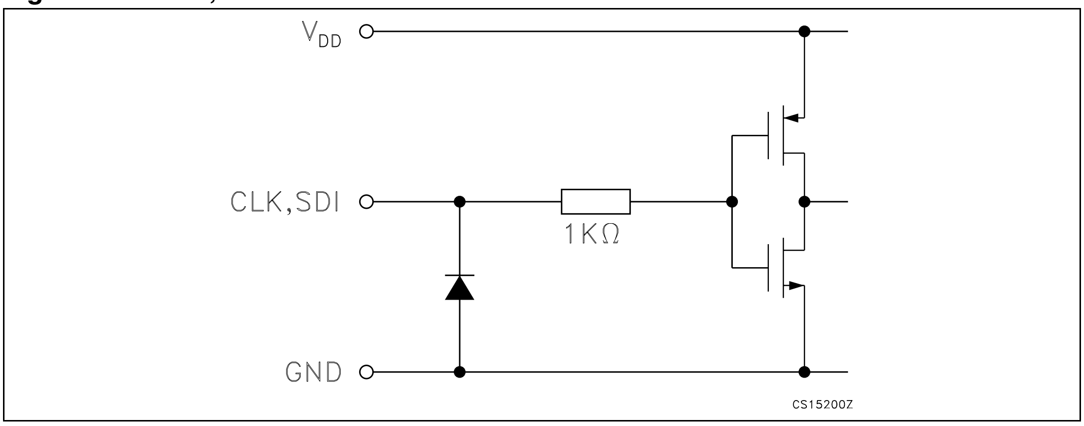


Figure 6. SDO terminal

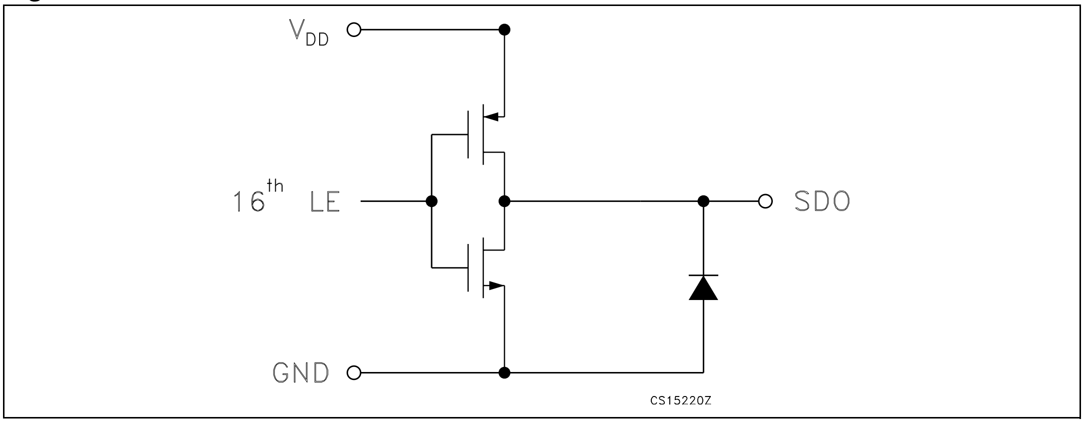
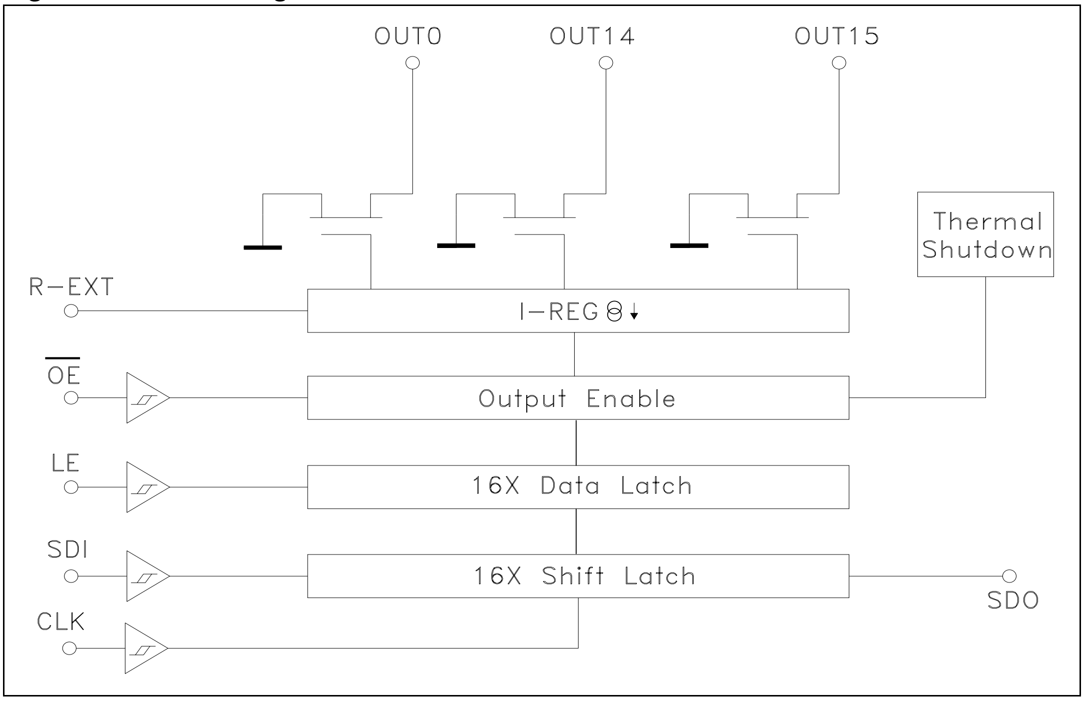


Figure 7. Block diagram



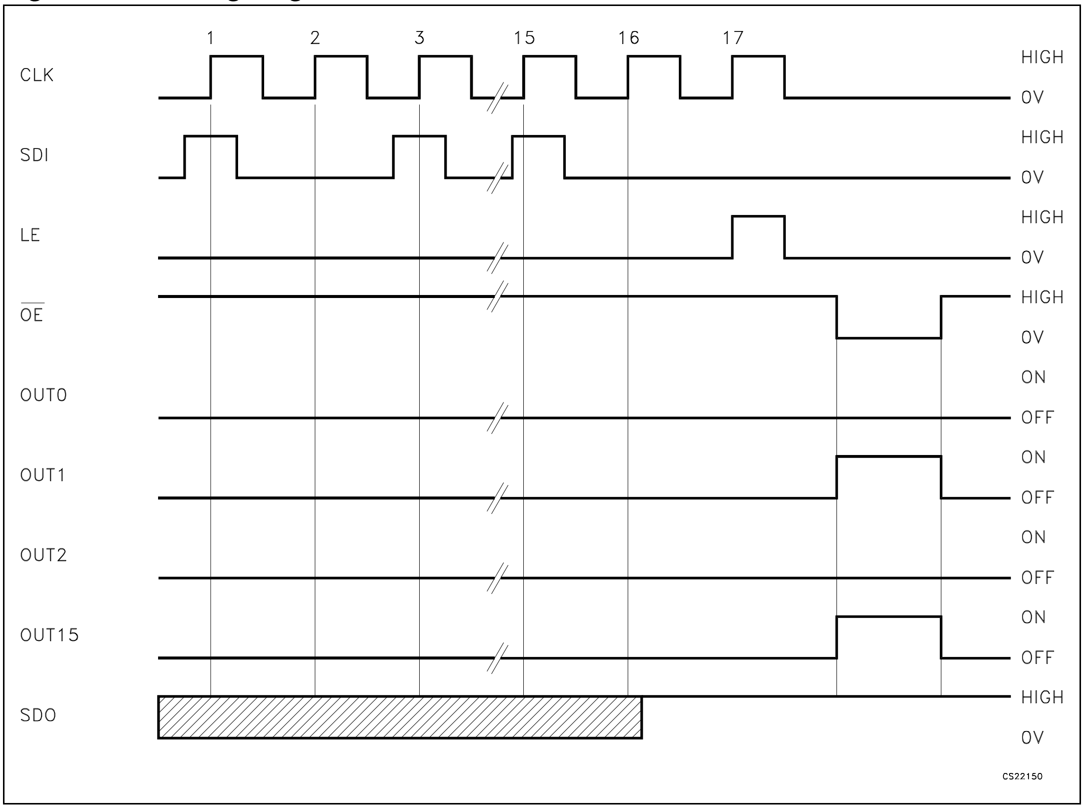
5 Timing diagrams

Table 9. Truth table

CLOCK	LE	$\overline{OE}$	Serial-IN	OUT0 .... OUT7 .... OUT15	SDO
↑	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
↑	L	L	Dn + 1	No change	Dn - 14
↑	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
↓	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
↓	X	H	Dn + 3	OFF	Dn - 13

Note: OUTn = ON when Dn = H OUTn = OFF when Dn = L

Figure 8. Timing diagram



Note: The latches circuit holds data when the LE terminal is Low.

1. *When LE terminal is at high level, latch circuit does not hold the data it passes from the input to the output.*
2. *When $\overline{OE}$ terminal is at low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.*
3. *When $\overline{OE}$ terminal is at high level, it switches off all the data on the output terminal.*

Figure 9. Clock, serial-in, serial-out

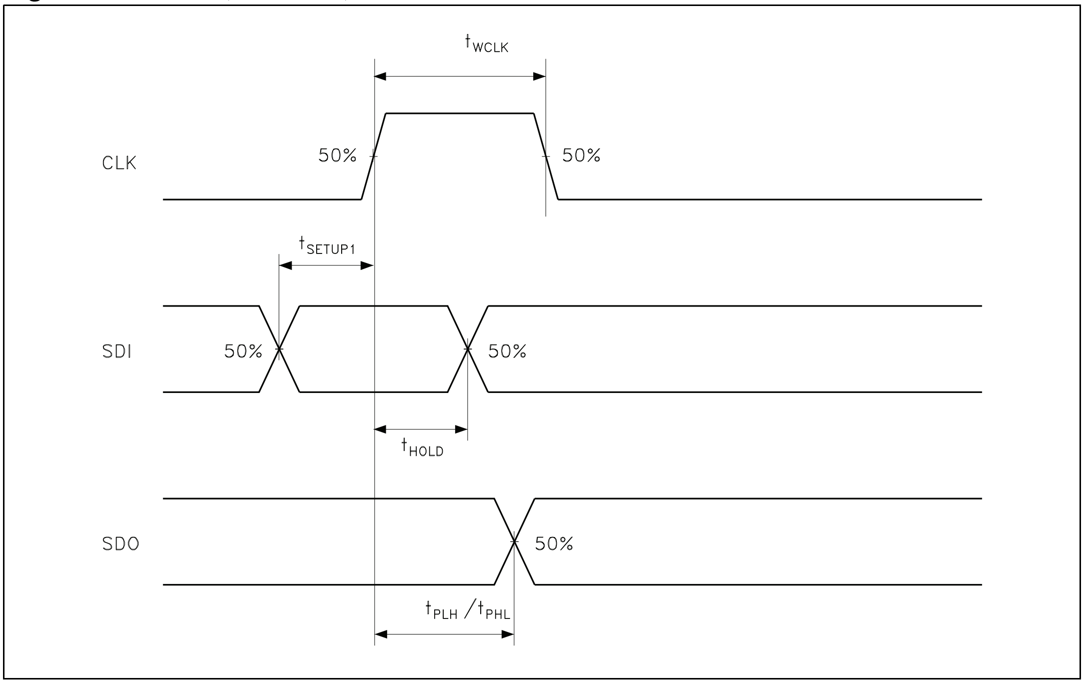


Figure 10. Clock, serial-in, latch, enable, outputs

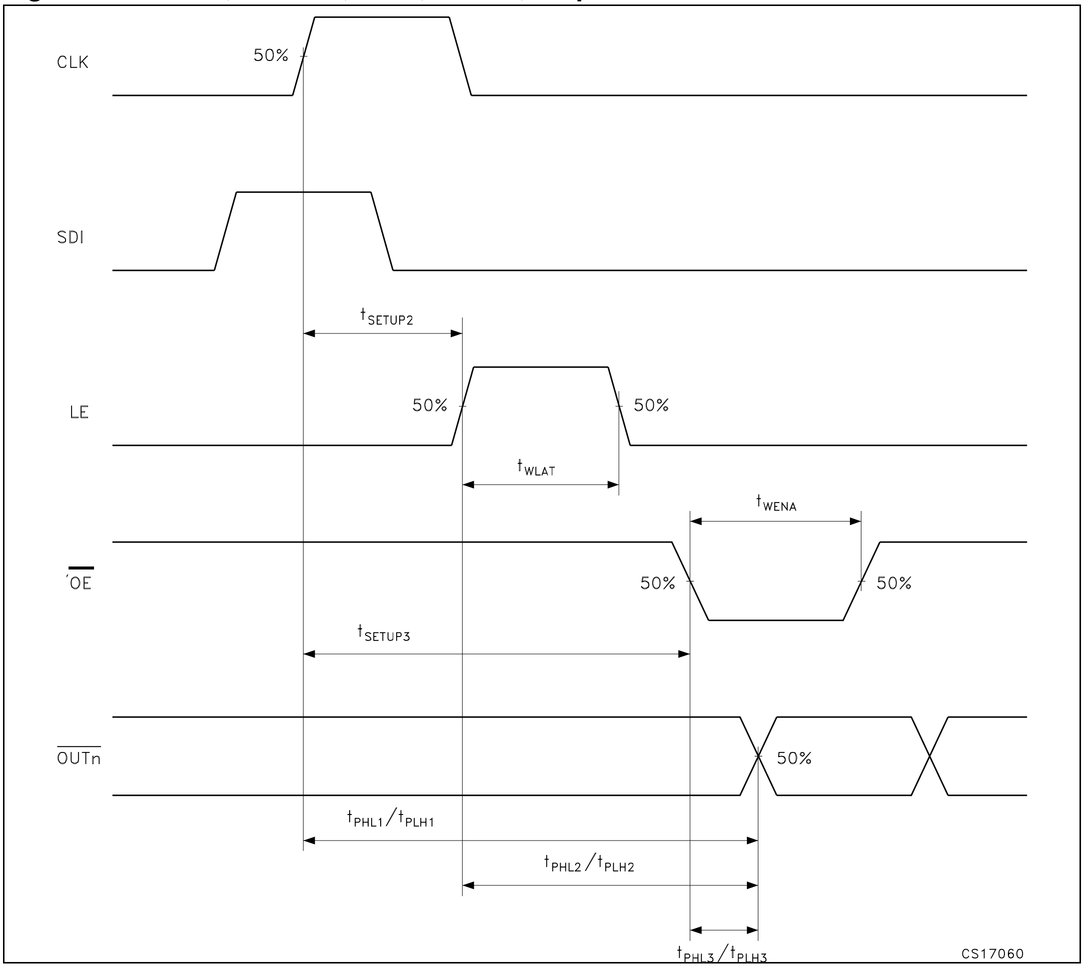
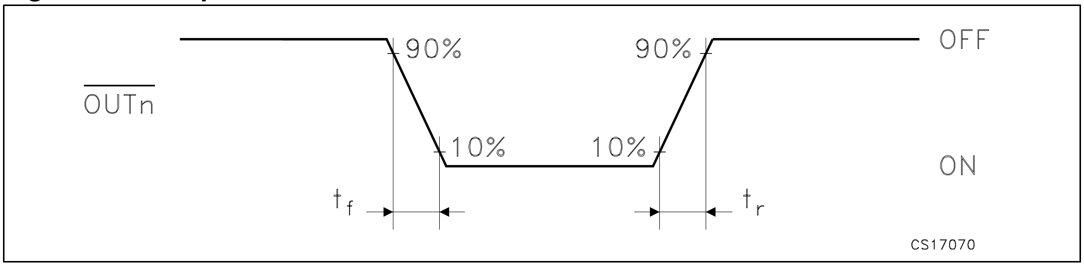


Figure 11. Outputs



6 Typical characteristics

Figure 12. Output current-R_{EXT} resistor

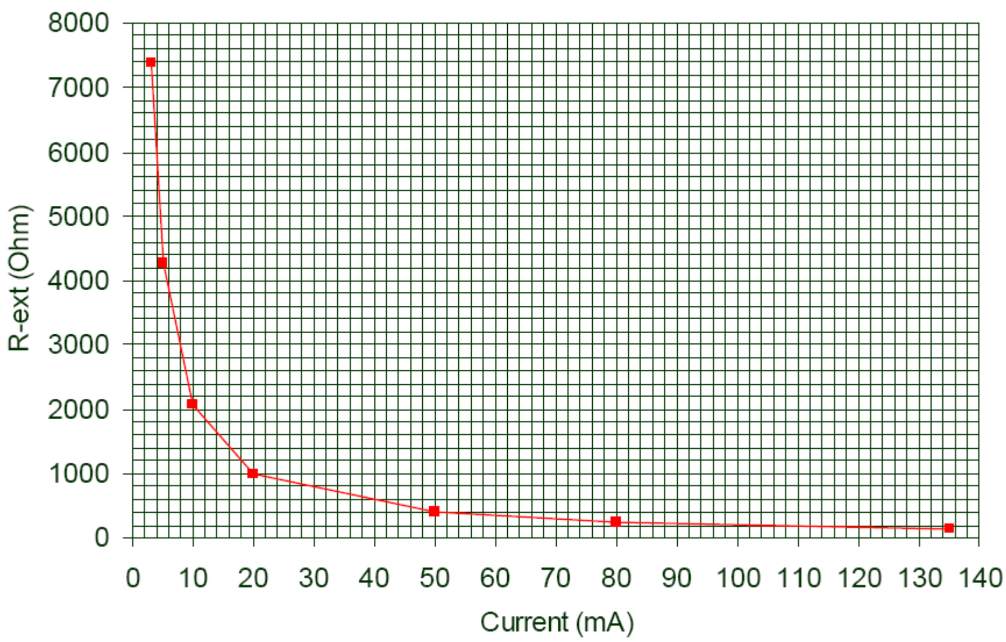


Table 10. Output current-R_{EXT} resistor

Rext (Ω)	Output current (mA)
7370	3
4270	5
2056	10
1006	20
382	50
251	80
200	100

Figure 13. Output current vs $\pm \Delta I_{OL}(\%)$ $T_A = 25$ °C

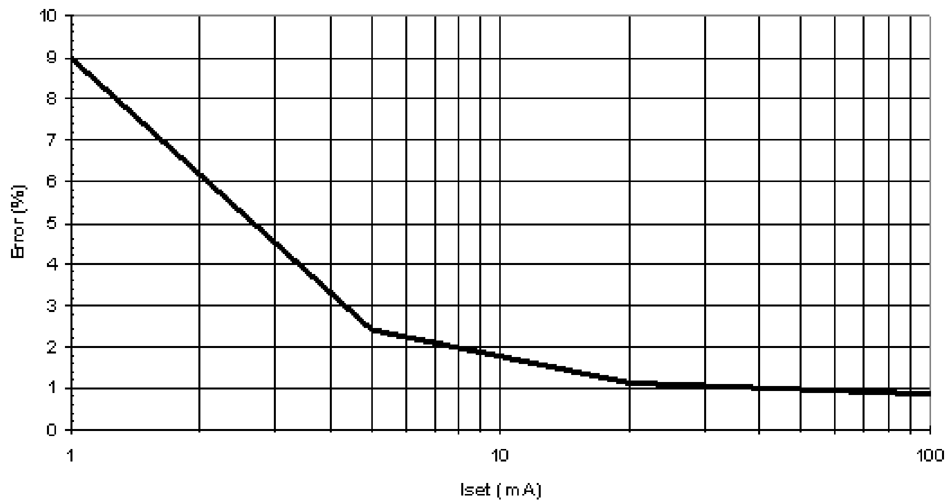
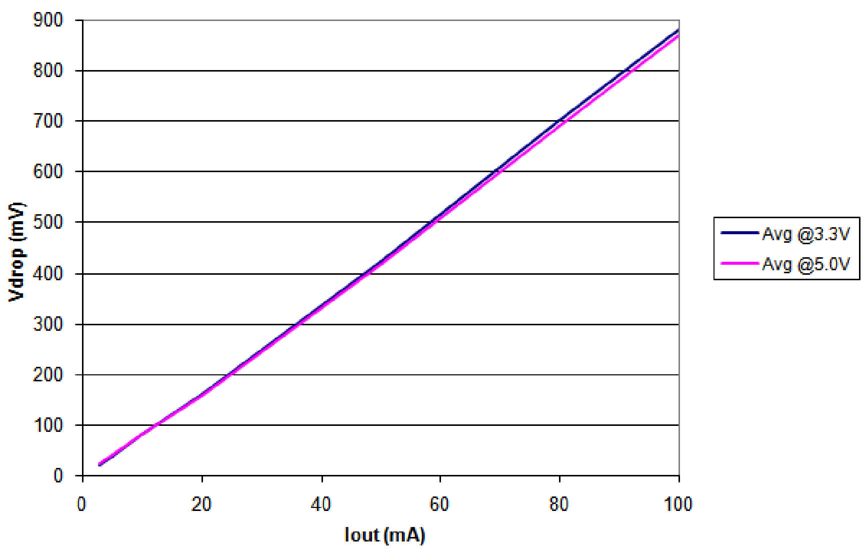
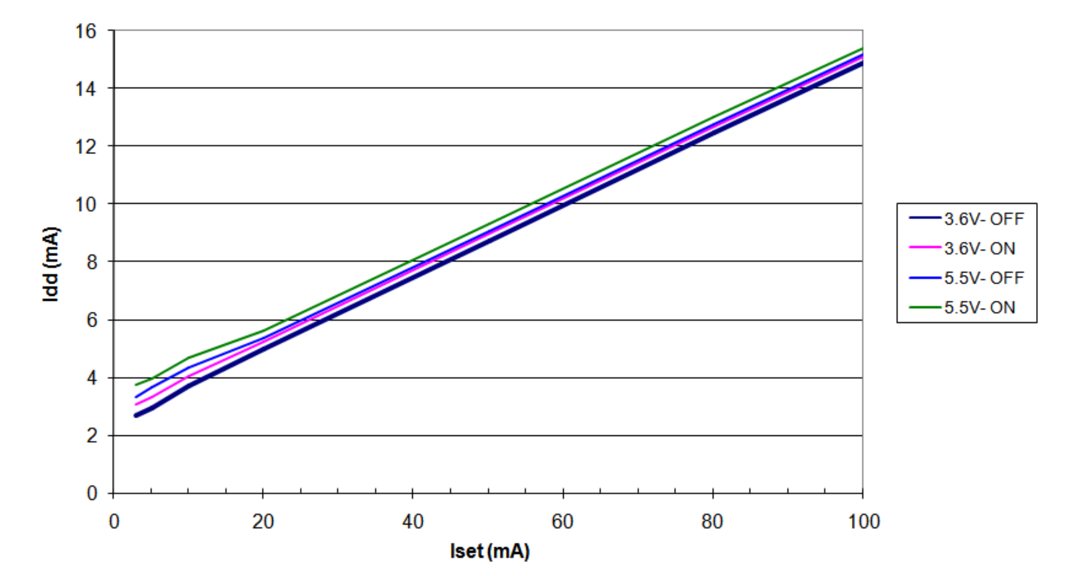


Figure 14. I_{SET} vs drop out voltage (V_{drop}) $T_A = 25$ °C



Iout (mA)	Avg @3.3 V	Avg @5.0 V
3	20	22
5	37	40
10	79	79
20	160	158
50	422	415
80	700	690
100	880	870

Figure 15. I_{DD} ON/OFF, T_A = 25 °C



7 Test circuit

Figure 16. DC characteristic

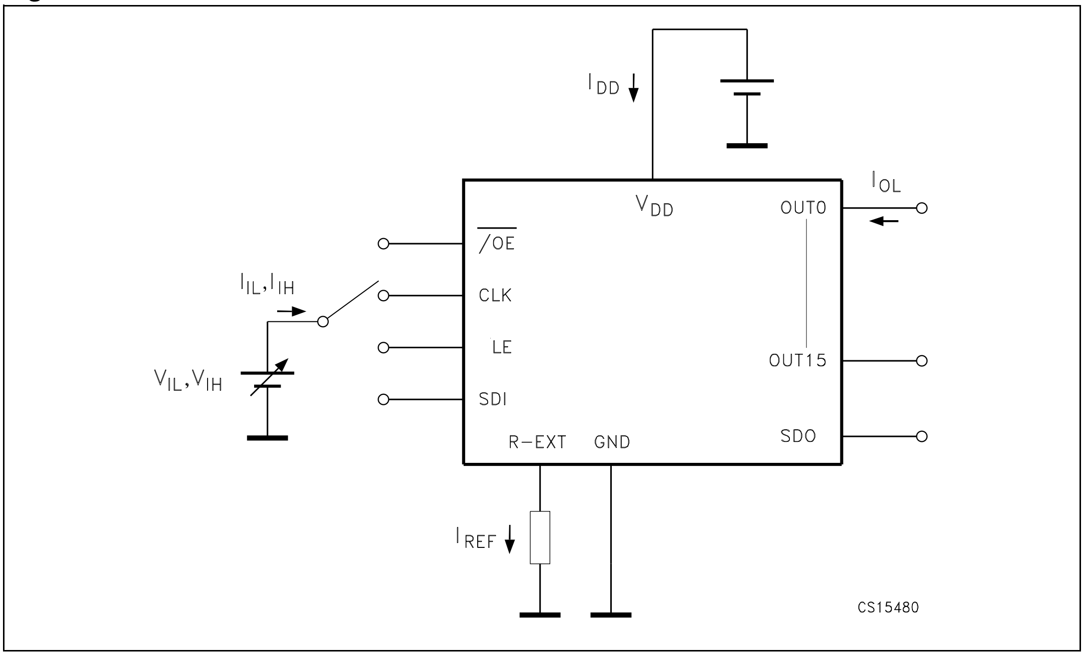


Figure 17. AC characteristic

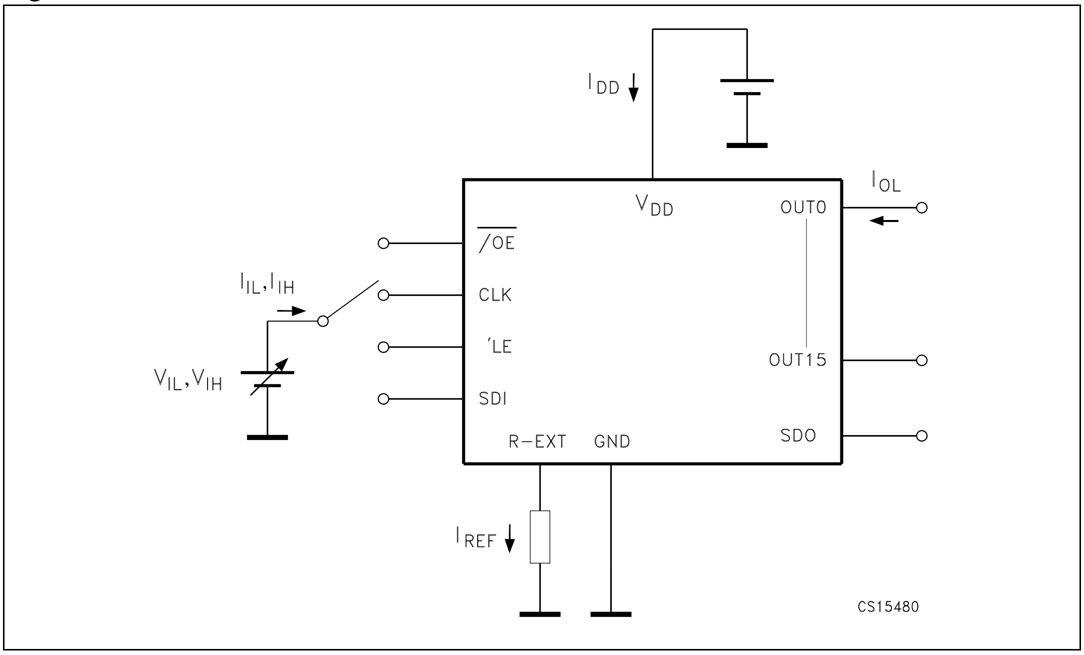
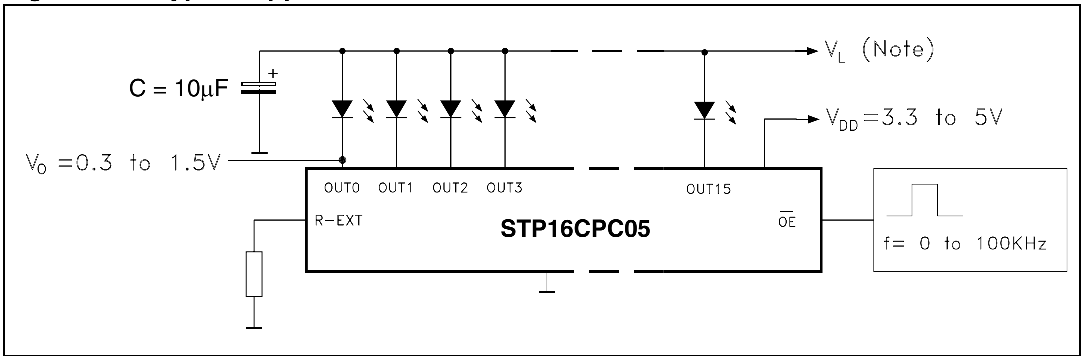


Figure 18. Typical application schematic



Note: *V_L will be determined by the V_F of the LEDs*

Test condition: Temp. = 25 °C, V_{DD} = 3.3 V, C_L = 10 pF, Freq. = 1 MHz,

Figure 19. Turn ON output current setup

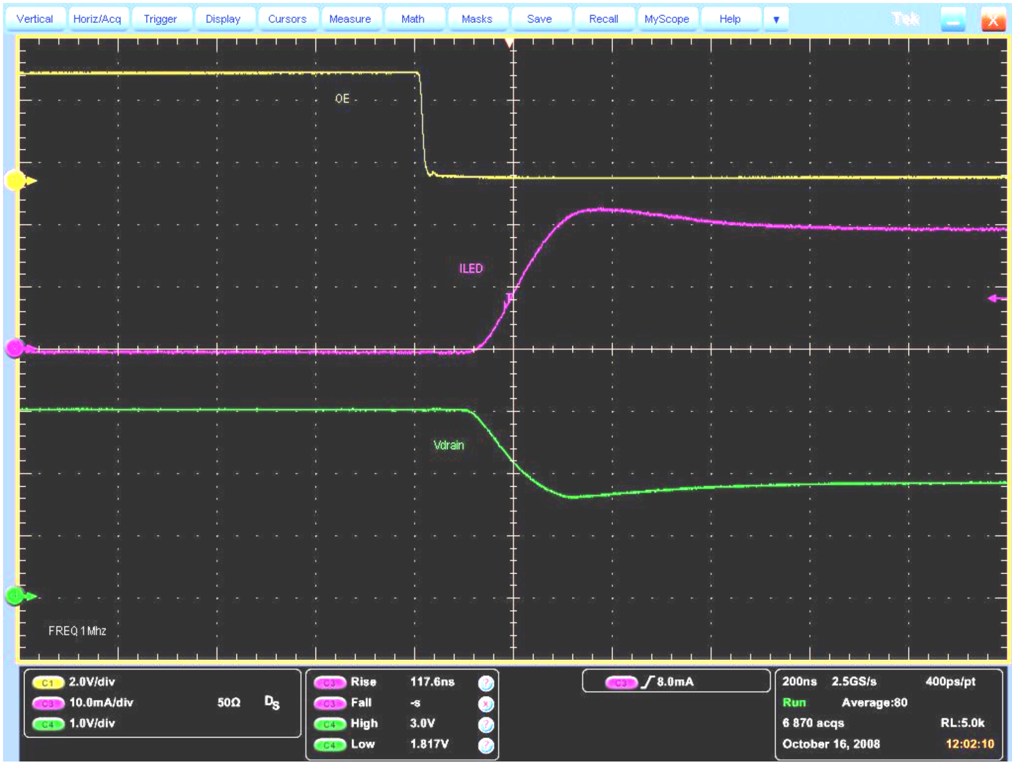


Figure 20. Turn OFF output current setup



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 11. QSOP-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.54	1.62	1.73	0.061	0.064	0.068
A1	0.1	0.15	0.25	0.004	0.006	0.010
A2		1.47			0.058	
b	0.31	0.2		0.012	0.008	
c	0.254	0.17		0.010	0.007	
D	8.56	8.66	8.76	0.337	0.341	0.345
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.91	4.01	0.150	0.154	0.158
e		0.635			0.025	
L	0.4	0.635	0.89	0.016	0.025	0.035
h	0.25	0.33	0.41	0.010	0.013	0.016
<	8°	0°				

Figure 21. QSOP-24 package dimensions

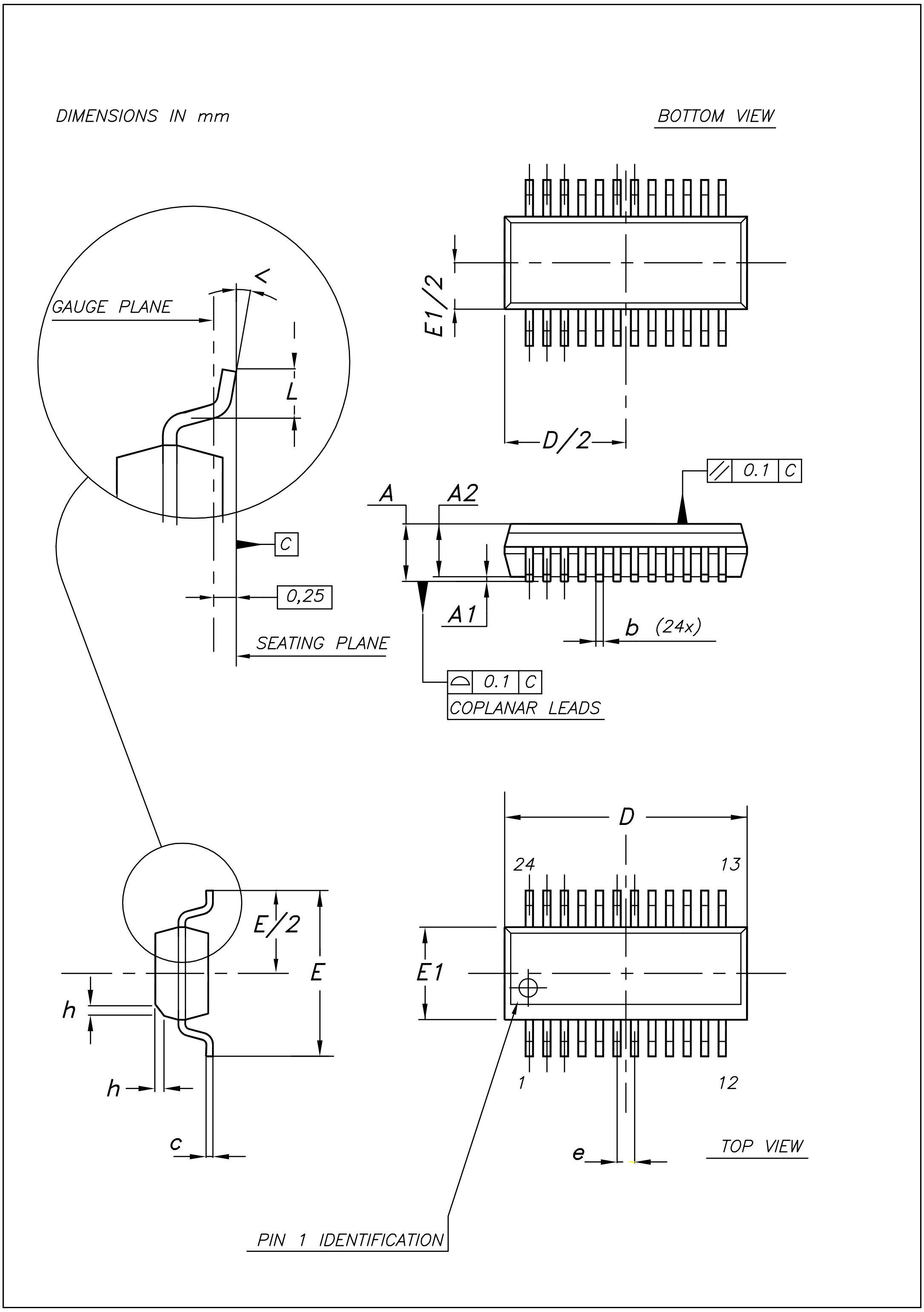


Table 12. TSSOP24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

Figure 22. TSSOP24 package dimensions

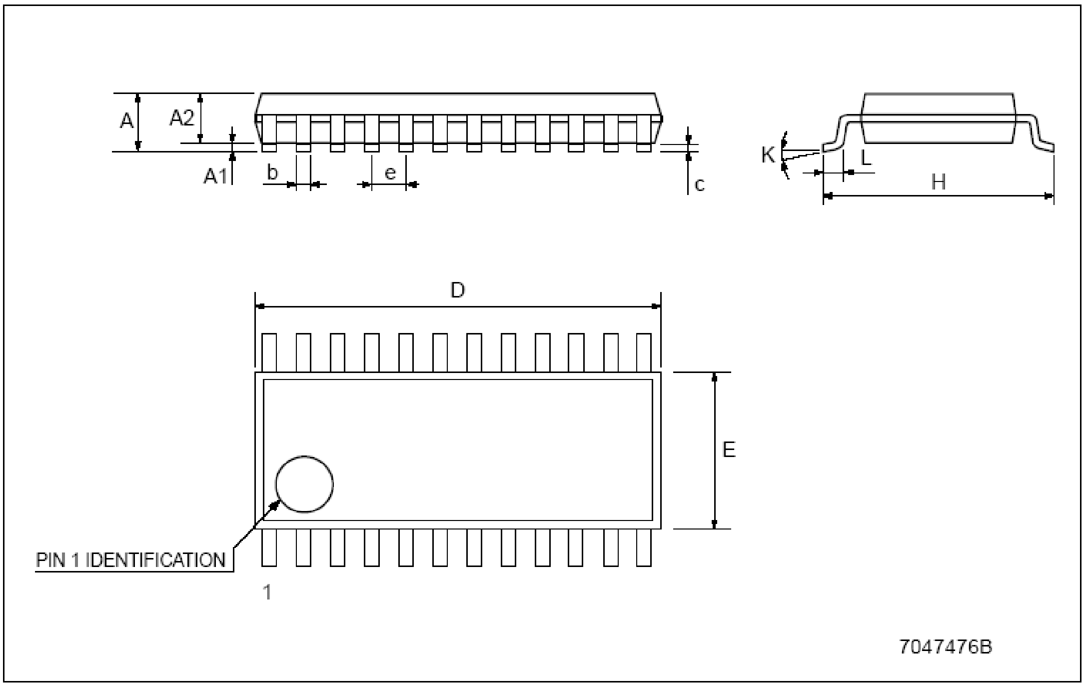


Table 13. Tape and reel TSSOP24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A		-	330		-	12.992
C	12.8	-	13.2	0.504	-	0.519
D	20.2	-		0.795	-	
N	60	-		2.362	-	
T		-	22.4		-	0.882
Ao	6.8	-	7	0.268	-	0.276
Bo	8.2	-	8.4	0.323	-	0.331
Ko	1.7	-	1.9	0.067	-	0.075
Po	3.9	-	4.1	0.153	-	0.161
P	11.9	-	12.1	0.468	-	0.476

Figure 23. Reel dimensions

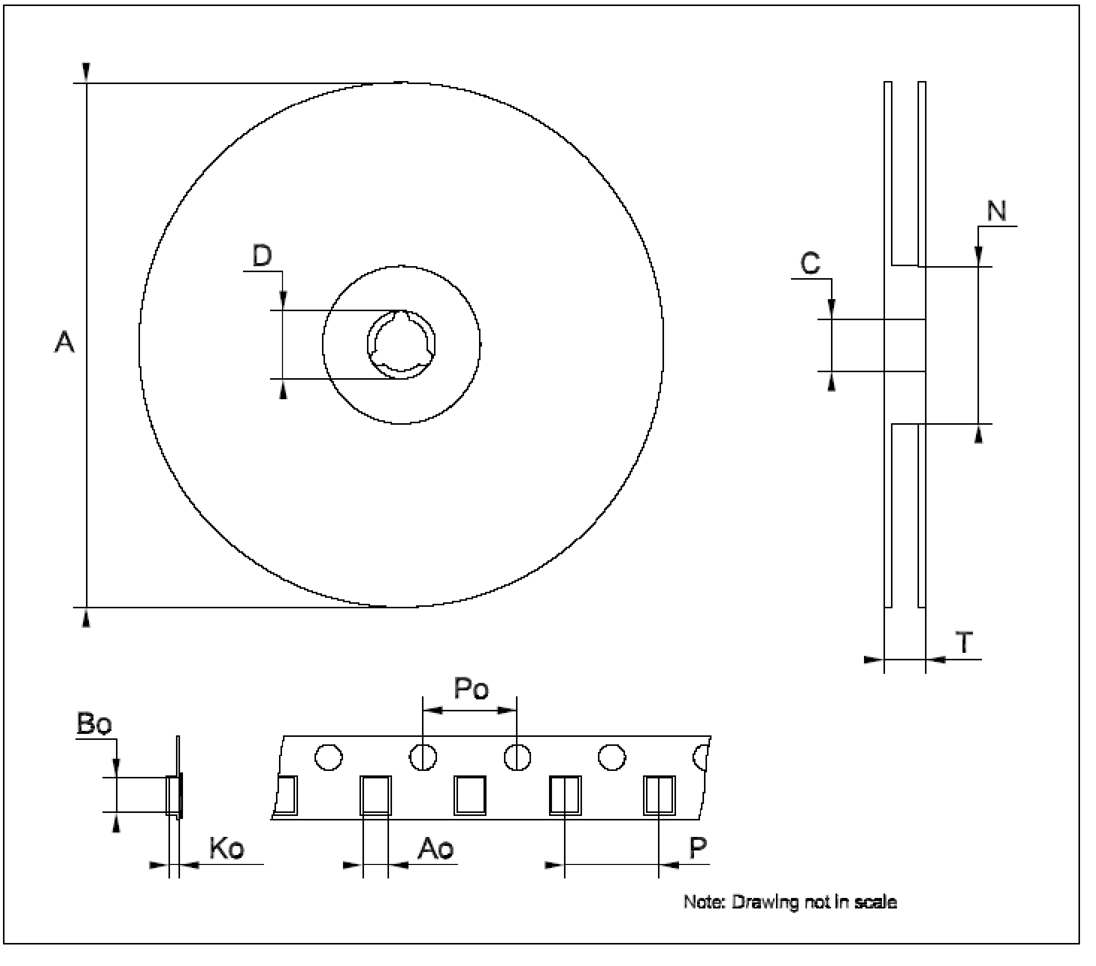


Table 14. SO-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 24. SO-24 package dimensions

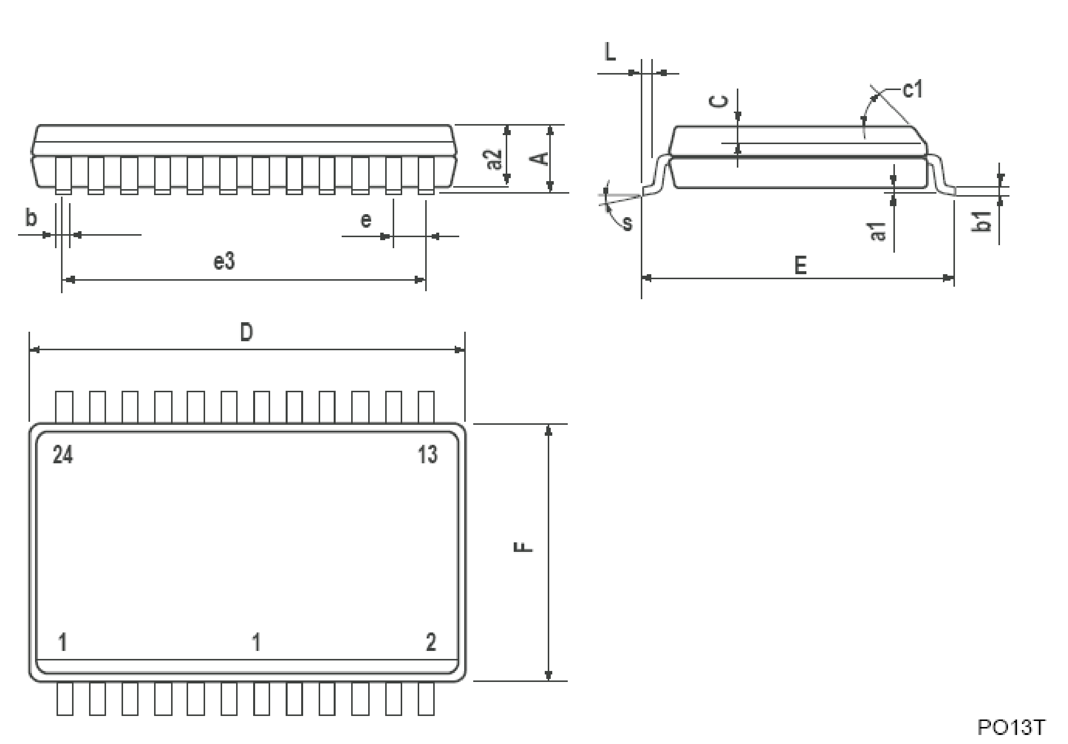


Table 15. Tape and reel SO-24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A		-	330		-	12.992
C	12.8	-	13.2	0.504	-	0.519
D	20.2	-		0.795	-	
N	60	-		2.362	-	
T		-	30.4		-	1.197
Ao	10.8	-	11.0	0.425	-	0.433
Bo	15.7	-	15.9	0.618	-	0.626
Ko	2.9	-	3.1	0.114	-	0.122
Po	3.9	-	4.1	0.153	-	0.161
P	11.9	-	12.1	0.468	-	0.476

Figure 25. Reel dimensions

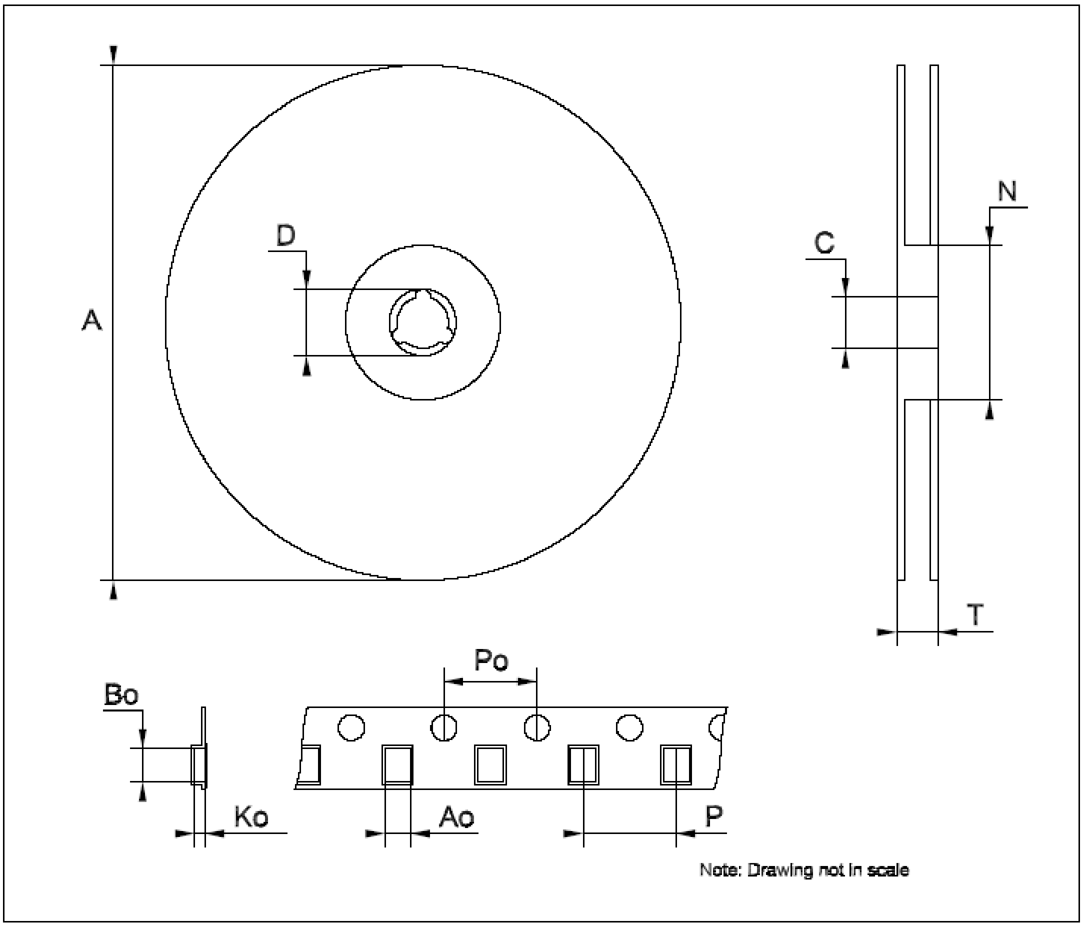
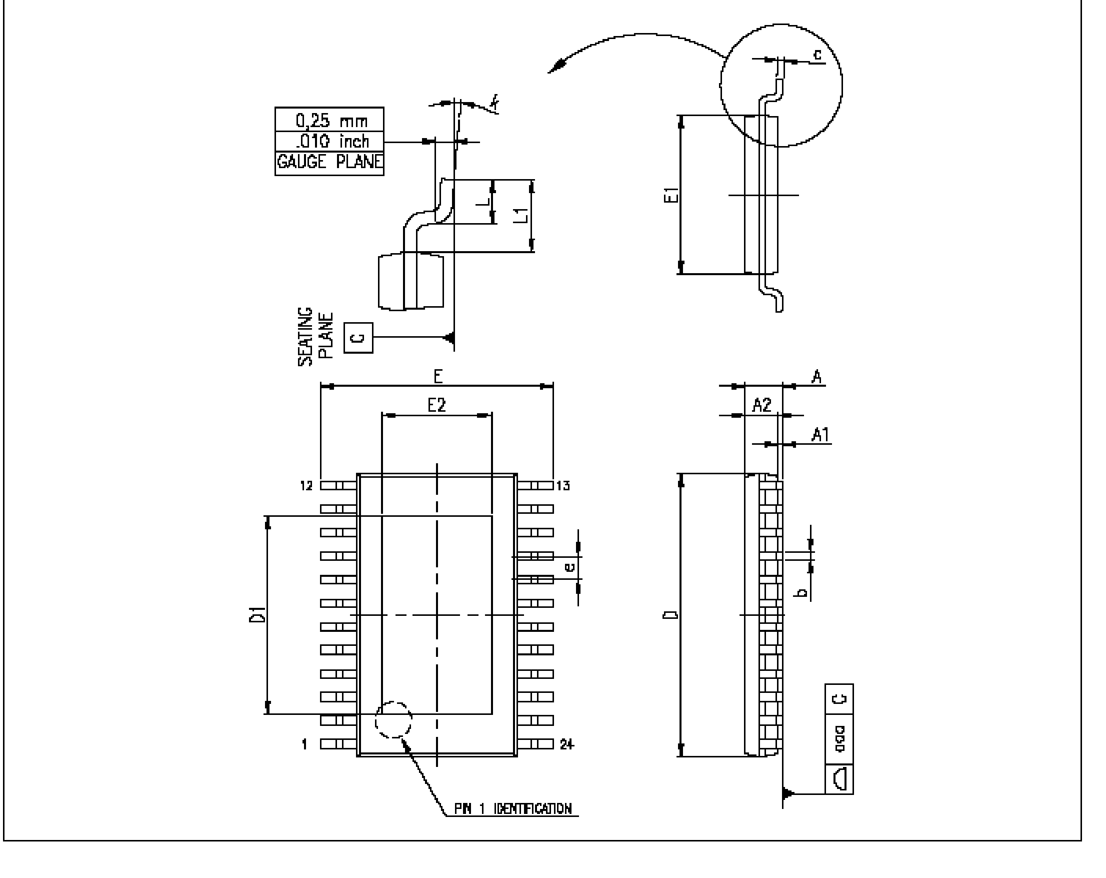


Table 16. TSSOP24 exposed-pad

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1	4.7	5.0	5.3	0.185	0.197	0.209
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.2	3.5	0.114	0.126	0.138
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 26. TSSOP24 dimensions



9 Revision history

Table 17. Document revision history

Date	Revision	Changes
30-Jan-2009	1	First release
12-May-2009	2	Updated *Table 6 on page 5*
29-Oct-2009	3	Updated *Note: on page 3*

Please Read Carefully: